**IN THE CLAIMS**

1-11. (Cancelled)

12. (Previously presented) A semiconductor device having multi-layered interconnection lines, the semiconductor device comprising:

lower interconnection lines disposed on a semiconductor substrate, the lower interconnection lines substantially coplanar, the lower interconnection lines aligned in a first direction and disposed parallel to one another, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, an end of the first lower interconnection line and an end of the second lower interconnection line disposed a substantially equal distance away from an end of the third lower interconnection line;

an interlayer insulating layer disposed on a surface of the substrate having the lower interconnection lines; and

upper interconnection lines disposed on the insulating layer, the upper interconnection lines substantially coplanar, the upper interconnection lines aligned in the first direction and disposed parallel to each other, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line, wherein the width of the upper interconnection lines is less than the width of the lower interconnection lines.

13. (Original) The semiconductor device of claim 12, further comprising:

a fourth upper interconnection line formed on the insulating layer and located on the same line as the third upper interconnection line but separated from it by a distance, the distance between the third and fourth upper interconnection lines being greater than a longest foeus distance.

14. (Original) The semiconductor device of claim 12, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

15. (Previously presented) The semiconductor device of claim 12, wherein the interlayer insulating layer comprises at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

16. (Original) The semiconductor device of claim 12, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

17-22. (Cancelled)

23. (Previously presented) A semiconductor device comprising:

lower interconnection lines, the lower interconnection lines substantially coplanar and disposed parallel to each other on a semiconductor substrate, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower interconnection line;

an interlayer insulating layer disposed on a surface of the substrate having the lower interconnection lines; and

upper interconnection lines, the upper interconnection lines substantially coplanar and disposed parallel to each other on the insulating layer, the upper interconnection lines disposed parallel to and aligned in the same direction as the lower interconnection lines, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line between the first and second upper interconnection lines, wherein the width of the upper interconnection lines is less than the width of the lower interconnection lines.

24. (Currently amended) The semiconductor device of claim 23, the upper interconnection lines further comprising a fourth upper interconnection line disposed parallel to the first and the second upper interconnection lines~~, the fourth upper interconnection line further disposed such that a vertical plane running along the length of the third upper interconnection line and the fourth upper interconnection line bisects the third upper interconnection line and the~~

~~fourth upper interconnection line~~, wherein an end of the third upper interconnection line and an end of the fourth upper interconnection line separated from each other by a distance that is greater than a longest focus distance.

25. (Previously presented) The semiconductor device of claim 23, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

26. (Previously presented) The semiconductor device of claim 23, wherein the interlayer insulating layer comprises at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

27. (Previously presented) The semiconductor device of claim 23, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

28. (Currently amended) A semiconductor device comprising:

lower interconnection lines disposed parallel to each other on a semiconductor substrate, the lower interconnection lines including a first lower interconnection line, a second lower interconnection line, and a third lower interconnection line between the first and second lower interconnection lines, the first and second lower interconnection lines extending past an end of the third lower interconnection line;

an interlayer insulating layer disposed on a surface of the substrate having the lower interconnection lines, wherein a top surface of the interlayer insulating layer includes a plurality of sloped surfaces corresponding to the first, second, and third lower interconnection lines, wherein a focus area is defined over the plurality of sloped surfaces; and

upper interconnection lines disposed parallel to each other on the top surface of the insulating layer, the upper interconnection lines including a first upper interconnection line, a second upper interconnection line, and a third upper interconnection line between the first and second upper interconnection lines, the first, second, and third upper interconnection lines ~~aligned with~~ overlapping the first, second, and third lower interconnection lines, respectively,

wherein the third upper interconnection line is outside the focus area ~~such that a first vertical plane running along the length of the first lower interconnection line and the first upper interconnection line bisects the first lower interconnection line and the first upper interconnection line, a second vertical plane running along the length of the second lower interconnection line and the second upper interconnection line bisects the second lower interconnection line and the second upper interconnection line, and a third vertical plane running along the length of the third lower interconnection line and the third upper interconnection line bisects the third lower interconnection line and the third upper interconnection line~~.

29. (Currently amended) The semiconductor device of claim 28, the upper interconnection lines further comprising a fourth upper interconnection line disposed parallel to the third upper interconnection line and between the first and second upper interconnection lines ~~that is also bisected in a lengthwise direction by the third vertical plane~~, an end of the fourth upper interconnection line and an end of the third upper interconnection line separated from each other by a distance that is greater than a longest focus distance.

30. (Previously presented) The semiconductor device of claim 28, wherein the lower interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

31. (Previously presented) The semiconductor device of claim 28, wherein the interlayer insulating layer comprises at least one layer selected from the group consisting of BPSG, USG, PSG, SOG and PE-TEOS.

32. (Previously presented) The semiconductor device of claim 28, wherein the upper interconnection lines comprise a layer chosen from the group consisting of a poly-silicon layer, a silicide layer, and a metal layer.

33. (Previously presented) The semiconductor device of claim 12, wherein the upper interconnection lines and the lower interconnection lines are disposed such that a vertical projection of each of the first upper interconnection line, second upper interconnection line, and

third interconnection line on upper surfaces of the first lower interconnection line, second lower interconnection line, and third lower interconnection line, respectively, lies within the boundaries defined by the upper surfaces of the first lower interconnection line, the second lower interconnection line, and the third lower interconnection line, respectively.

34. (Previously presented) The semiconductor device of claim 23, wherein the lengths of the upper interconnection lines and the lengths of the lower interconnection lines are aligned in the same direction.

35. (New) The semiconductor device of claim 28, wherein the upper interconnection lines are disposed directly on the top surface of the insulating layer.